

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Seitz, et al.
Serial No. : To Be Assigned
Filed : February 11, 2004.
For : DRAM WITH VERY SHALLOW TRENCH ISOLATION
Examiner : To be assigned
Group Art Unit : To be assigned

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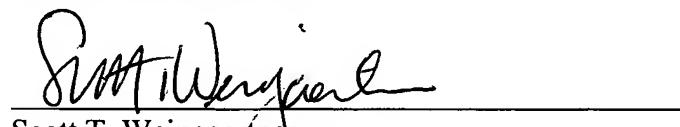
Sir:

Applicant submits this communication in compliance with 37 C.F.R. §§1.56, 1.97 and 1.98. Attached to this communication are Form PTO/SB/08A and PTO/SB/08B, identifying the publications for which consideration is requested. Copies of the references are enclosed.

This Information Disclosure Statement is being filed concurrently with a new patent application and therefore no fee should be required. However, should it be determined that any fees are due in connection with this communication, authorization is hereby given to charge Deposit Account No. 23-1703.

Dated: February 11, 2004

Respectfully submitted,



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U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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Sheet	2	of	2	Attorney Docket Number	1115747-0002//2002P50545US

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
		U. GRUENING, et al, "A Novel Trench DRAM Cell with a VERTical Access Transistor and Buried STrap (VERI BEST) for 4Gb/16Gb," 0-7803-5413-3/99, 1999 IEEE, pp. 1-4.		
		W. NEUMUELLER, et al., "DRAM Technology For Today's Market And Future DRAM Generations," pp. 1-8.		
		C.J. RADENS, "An Orthogonal 6F ² Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM," 0-7803-6441-4/00 2000 IEEE, pp. 1-4.		

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